

1. A method of forming a multi-level, multi-bit stacked gate flash memory cell comprising the steps of:

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providing a substrate having a first dielectric layer formed thereon;

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forming a second dielectric layer over said first dielectric layer;

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forming an opening in said second dielectric layer;

12 forming floating-gate spacers inside said opening;

forming a third dielectric layer over said floating-gate spacers;

forming a control gate over said conformal dielectric layer;

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removing said second dielectric layer adjacent said opening, thus leaving a stand-alone cell structure comprising said floating gate spacers and said control gate separated by intervening said third dielectric layer; and

24 forming insulative spacers on the outside walls of said cell

structure in completion of said multi-level stacked gate flash memory cell.

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2. The method of claim 1, wherein said second dielectric layer comprises nitride formed by CVD at a temperature between about 300 to 700°C by reacting dichlorosilane ( $\text{SiCl}_2\text{H}_2$ ) with ammonia ( $\text{NH}_3$ ).

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3. The method of claim 1, wherein said second dielectric layer has a thickness between about 1200 to 2500 Å.

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4. The method of claim 1, wherein said forming said floating-gate spacers comprise polysilicon formed by using LPCVD at a temperature between about 300 to 700°C and then anisotropic etching of said first polysilicon to form spacers.

5. The method of claim 1, wherein said third dielectric layer is (oxide-nitride-oxide) ONO having a thickness between about 600 to 1100°C.

6. The method of claim 1, wherein said forming said control gate comprises polysilicon layer formed with silicon source  $\text{SiH}_4$  using LPCVD at a temperature between about 300 to 700 °C.

7. A method of forming a multi-level, multi-bit stacked gate flash memory cell comprising the steps of:

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providing a substrate having gate oxide formed thereon and shallow trench and P-well formed therein;

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forming nitride layer over said substrate;

9 patterning a self-aligned gate to form an opening in said nitride layer;

12 forming a first oxide layer over said substrate including said opening;

15 forming first oxide spacers in said opening;

performing floating source implant in said substrate through  
18 said opening;

removing said first oxide spacers in said opening;

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forming a first polysilicon layer over said substrate including said opening in said nitride layer;

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forming first polysilicon floating-gate spacers on the vertical walls of said opening in said nitride layer;

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forming a conformal dielectric layer over said substrate including said first polysilicon floating-gate spacers and

30 the bottom of said opening;

forming second polysilicon layer over said substrate

33 including said opening;

removing said second polysilicon layer until said conformal

36 dielectric layer over said opening is reached, thus leaving said second polysilicon in said opening as a control gate therebetween said floating-gate spacers with intervening

39 said conformal dielectric layer;

removing said conformal dielectric layer adjacent said

42 opening and said nitride layer underlying said dielectric layer;

45 performing mildly doped drain implant to form the drain of said stacked gate cell;

48 forming a second dielectric layer over said substrate  
including said opening; and

51 forming second dielectric spacers on the outside vertical  
walls of said floating gate spacers to complete the forming  
of said multi-level stacked gate flash memory cell.

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8. The method of claim 7, wherein said forming said nitride  
layer is accomplished by CVD at a temperature between about  
3 300 to 700°C by reacting dichlorosilane ( $\text{SiCl}_2\text{H}_2$ ) with  
ammonia ( $\text{NH}_3$ ).

9. The method of claim 7, wherein said nitride layer has a  
thickness between about 1200 to 2500 Å.

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10. The method of claim 7, wherein said floating source  
implant is accomplished with As ions at a dosage level  
3 between about  $1 \times 10^{14}$  to  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and at an energy  
between about 5 to 40 KEV.

11. The method of claim 7, wherein said forming said first  
polysilicon layer is accomplished with silicon source  $\text{SiH}_4$   
3 using LPCVD at a temperature between about 300 to 700°C.

12. The method of claim 7, wherein said forming said conformal dielectric layer is accomplished by depositing ONO  
3 at a temperature between about 600 to 1100 °C.

13. The method of claim 7, wherein said conformal dielectric layer has a thickness between about 150 to 250 Å.  
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14. The method of claim 7, wherein said forming said second polysilicon layer is accomplished with silicon source  $\text{SiH}_4$   
3 using LPCVD at a temperature between about 300 to 700°C.

15. The method of claim 7, wherein said second polysilicon layer has a thickness between about 1500 to 3000 Å.  
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16. The method of claim 7, wherein said removing said second polysilicon layer is accomplished by chemical-  
3 mechanical polishing (CMP).

17. The method of claim 7, wherein said performing said medium doped drain implant is accomplished with As ions at a  
3 dosage level between about  $1 \times 10^{14}$  to  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and at an energy between about 10 to 60 KEV

18. The method of claim 7, wherein said second dielectric layer has a thickness between about 1500 to 3000 Å.

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19. A multi-level, multi-bit stacked gate flash memory cell structure comprising:

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floating gate spacers having convex walls facing each other, and vertical outside walls;

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a conformal dielectric layer covering said convex walls of said floating gate spacers;

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a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer; and

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insulative spacers formed on said vertical outside walls of said floating gates.

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20. The stacked gate flash memory cell of claim 19, wherein said floating gate spacers comprise polysilicon having a lateral thickness between about 500 to 2000 Å.

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21. The stacked gate flash memory cell of claim 19, wherein said conformal dielectric layer comprises oxide-nitride-oxide (ONO) having a thickness between about 600 to 1100 Å.

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22. The stacked gate flash memory cell of claim 19, wherein said control gate comprises polysilicon.

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23. The stacked gate flash memory cell of claim 19, wherein said oxide spacers have a lateral thickness between about 3 1000 to 3000 Å.